FORM PTO-1449 (10-96 MODIFIED)
LIST OF PUBLICATIONS FOR APPLICANT'S
INFORMATION DISCLOSURE STATEMENT

Substitute for form 1449A/PTO				*Complete if Known*	
				Application Number	~~Not Yet Assigned~~ 10/806,680
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date	March 22, 2004
				First Named Inventor	Narain D. Arora
				Group Art Unit	~~Not Yet Assigned~~ 2825
(use as many sheets as necessary)				Examiner Name	~~Not Yet Assigned~~ LIN, SUN J.
Sheet	1	of	2	Attorney Docket Number	700693-4026

U.S. PATENT DOCUMENTS						
Examiner Initials*		Document No.	Date	Name of Patentee or Applicant	Class/SubClass	Filing Date (if appropriate)
	AA	5,999,010	12/07/1999	Narain D. Arora, et. al.	324/765	12/08/1997
	AB	6,291,254	09/18/2001	Shih-tsun Alexander Chou	438/18	02/04/1999
	AC	6,312,963	11/06/2001	Shih-Tsun Alexander Chou	438/18	02/04/1999

FOREIGN DOCUMENTS							
Examiner Initials*		Document No.	Publication Date	Country	Class/SubClass	Translation	
						Yes Abstract	No
						☐	☐
						☐	☐

OTHER DOCUMENTS		
Examiner Initials*		Author, Title, Date, Pertinent Pages, Etc.
	CA	N.D Arora, L. Song, S. Shah, K. Joshi, K. Thumaty, A. Fujimura, J.P. Schoelkopf, H. Brut, M. Smayling, T. Nagata; Cadence Design Systems, San Jose, CA 95135; STMicroelectronics, Crolles, France, 38926; Applied Materials, Santa Clara, CA 95054; Test Chip Characterization Of X Architecture Diagonal Lines For Soc Design; 5 pages.
	CB	Narain D. Arora; Cadence Design Systems, Inc., San Jose, CA 95134, USA; Modeling And Characterization Of Copper Interconnects For Soc Design; 6 pages.
	CC	Dae-Hyung Cho, Man-Ho Seung, Nam-Ho Kim, and Hun-Sup Park; Measurement And Characterization Of Multi-Layered Interconnect Capacitance For Deep Submicron Vlsi Technology; 4 pages; Proc. IEEE 1997 Int. Conference on Microelectronic Test Structures, Vol, 10, March 1997.
	CD	James C. Chen, Dennis Sylvester, and Chenming Hu; An On-Chip, Interconnect Capacitance Characterization Method With Sub-Femto-Farad Resolution; 7 pages; Vol. 11, No. 2, May 1998.

OTHER DOCUMENTS		
Examiner Initials*		Author, Title, Date, Pertinent Pages, Etc.
	CE	Narain D. Arora and Li Song; Atto-Farad Measurement And Modeling Of On-Chip Coupling Capacitance; 1 of 3 pages; IEEE Electron Device Letters, IEEE Transactions on Semiconductor Manufacturing, Vol. 25, No. 2, February 2004.

Examiner Signature		Date Considered	11-21-05

* **EXAMINER**: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line though citation if not in conformance and not considered. Include copy of this form with next communication to applicant.